PROJECT PROFILE

2T104: Device and circuit performance boosted through silicon material fabrication (DECISIF)

TECHNOLOGY PLATFORM FOR NEXT-GENERATION CORE CMOS PROCESS

Partners:

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Project leader:

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Key project dates:

Start: 1 August 2008
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Countries involved:

France
Germany

The trend towards ultra thin body (UTB) devices now offers the most practical way to improve performance for specific technologies. In general, UTB devices fabricated with silicon-on-insulator (SOI) architectures make it possible to increase speed in high-performance applications such as microprocessors and memory chips. At the same time, it is possible to reduce energy consumption for low-power applications in handheld devices like mobile phones. Fully-depleted devices can be achieved either by using SOI material or through the silicon-on-nothing (SON) approach. Success in DECISIF will keep Europe in the global vanguard for core CMOS technology in both the high performance and low power areas.

As the limits of bulk silicon are being reached in the fabrication of ever faster and smaller electronic devices, new substrate materials are necessary to increase speeds and lower power consumption. Interest has focused on high mobility strained silicon and strained silicon-on-insulator (SOI) substrates with the intention of developing 300 mm wafers for full scale production

The MEDEA+ 2T104 DECISIF project set out to integrate performance boosters in fully and partially depleted SOI technologies for low power and high performance, to validate their impact by fabricating complex 45 nm node demonstrators directly comparable with bulk silicon and to develop design kits and SOI-adapted circuit design for evaluation by applications designers.

DECISIF bring together major European chipmakers, advanced substrate manufacturers and research centres with the overall objective of evaluating different substrate approaches and develop appropriate thin-film technologies. This work is essential to enable the manufacture of more powerful and lower-energy-consumption microprocessor and memory chips for portable devices such as laptops, mobile phones and MP3 players.

Demonstrating performance

Most of the work in DECISIF will be performed at 45 nm, the most advanced node available in Europe. Compared with previous projects that focused on materials and the evaluation of early devices, this new project will concentrate primarily on device and circuit demonstrations – including design, performance and yield as well as investigation of the best performance/cost compromises. While most of the emphasis is placed on device and circuit technology, several parallel substrate options will also be considered.

The use of strained SOI or hybrid orientation silicon wafers has already shown that device performance is enhanced by comparison with standard unstrained approaches. Systems developers will be able to adapt these benefits to their own needs and their own roadmaps with applications in various product families – including high-performance, low-power and radio frequency (RF) devices.

DECISIF offers a complete and innovative solution at substrate and device levels to meet the coming challenges of the International Technology Roadmap for Semiconductors (ITRS).

Addressing three objectives

Three specific objectives will be addressed:

1. Tackling **device issues** to determine the process modules to be developed for thin-film devices. This is the real core of the project where partners will be sharing basic technology developments so that they can be employed at a later stage when working at applications level. The project is intended to demonstrate the exceptional advantages of strained SOI material – including higher strain SOI material – at device level with channel material options for both N- and P-MOS technologies. It will also optimise and demonstrate the compatibility of source/drain stress or techniques with strained and unstrained material. Demonstrating the benefits of direct silicon bonded (DSB) material at device and circuit level for silicon-on-nothing technology will lead on to the process of characterising, modelling and maximising strain during device processing. Specific attention will be focused on the characterisation methods, which will be coupled with mechanical and technology computer-aided design (TCAD) simulations.
2. Focusing on **low power applications** to validate the developments performed at substrate and device levels. The aim here is to evaluate the impact of the advanced materials developed on the devices as well as on circuit performance and functionality. This will facilitate the demonstration of low power circuit functionality using thin-film technologies, as well as comparison with similar designs on bulk silicon. Evaluating early circuit yield on strained SOI material will provide a direct comparison with regular SOI substrates, while the evaluation of early circuit yield on DSB material will provide a direct comparison with bulk silicon substrates. Specific low power circuits will be designed and adapted for thin-film SOI and strained SOI technologies to evaluate the impact of strained material on circuit performance and density.
3. Developing a **partially depleted strained SOI technology** for high performance applications to demonstrate the advantages of strained SOI materials at device and circuit levels for partially-depleted SOI technology, while evaluating circuit yield on strained SOI material and providing feedback to the substrate development teams. This will also cover the correlation of strained SOI material quality in terms of defects, thickness uniformity and strain control, as well as circuit yield, make a comparison of various strained SOI processes and allow benchmarking with regular SOI substrates. Adapting the circuit design to take account of the performance improvement will facilitate evaluation of the impact of the circuit area.

Building up comparisons

DECISIF will gather a maximum of early technical information at integration level on a platform based on combining high mobility substrate materials and process-strained SOI architectures to assess better the tradeoffs of using global-strain and process-strain by comparison with competitive approaches such as process-strain only. The results of the present project will have to be compared with other benchmark approaches, not only in terms of technical results but also from an economic point of view.

This project supports European efforts to remain competitive in terms of core CMOS technology in both the high performance and low power areas. The acquisition of strategic industrial property related to such a new platform will enable Europe to maintain a strong position relative to aggressive players in the USA and Asia.

Over the past decade Europe has developed recognised leadership in SOI device technologies and substrate developments. This leadership needs to grow into a broader acceptance of the technology. Its introduction to both the high- and low-power markets should become widely accepted. In terms of the main semiconductor market, the memory sector is not being targeted at this stage. The benefit of such a project is to create and strengthen a complete ecosystem around SOI technology – substrate + process + device + characterisation + design + yield + manufacturing.

Application areas impacted by DECISIF cover a wide range of industrial and domestic equipment, including the 4G mobile market. The MEDEA+ project is also expected to strengthen the position of European chipmakers in thin-film SOI technologies, reinforcing their position in high and lower power applications. Direct and indirect employment opportunities are therefore bound to result.

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MEDEA+ Σ!2365 is the industry-driven pan-European programme for advanced co-operative R&D in microelectronics to ensure Europe's technological and industrial competitiveness in this sector on a worldwide basis.

MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon.